In the Claims:

Please amend the claims as follows:

1. (Previously Presented) A signal receiver inserted between a first and a second voltage reference and having a first and a second input terminal effective to receive differential signals and an output terminal effective to provide a converted signal, wherein the signal receiver comprises a conversion stage inserted between said first and second voltage references and connected between said first and second input terminals of said signal receiver and an input terminal of a hysteresis comparator, connected to said output terminal of said signal receiver, said conversion stage performing a conversion from any input signal received on respective input terminals to an intermediate signal provided on an output terminal and suitable for reception by said hysteresis comparator;

wherein the conversion stage further comprises:

a first current mirror connected to said first voltage reference and to said input terminals, as well as to a bias terminal;

a second current mirror connected to said second voltage reference and to said first input terminal, as well as to a circuit node;

a third current mirror connected to said second voltage reference and to said second input terminal, as well as to said output terminal; and

a fourth current mirror connected to said first voltage reference, to said circuit node, as well as to said output terminal.

2. (Previously Presented) A signal receiver according to claim 1, wherein said conversion stage performs an ALL-INPUT/single-ended conversion generating a trapezoidal signal.

3. (Previously Presented) A signal receiver according to claim 2, wherein said conversion stage is further connected to a bias terminal effective to receive a bias current.

4. (Previously Presented) A signal receiver inserted between a first and a second voltage reference and having a first and a second input terminal effective to receive differential signals and an output terminal effective to provide a converted signal, wherein the signal receiver comprises a conversion stage inserted between said first and second voltage references and connected between said first and second input terminals of said signal receiver and an input terminal of a hysteresis comparator, connected in turn to said output terminal of said signal receiver, said conversion stage performing a conversion from any input signal received on respective input terminals to an intermediate signal provided on an output terminal and suitable for reception by said hysteresis comparator;

wherein said conversion stage performs an ALL-INPUT/single-ended conversion generating a trapezoidal signal;

wherein said conversion stage is further connected to a bias terminal effective to receive a bias current; and

wherein said conversion stage comprises:

a first current mirror connected to said first voltage reference and to said input terminals, as well as to said bias terminal;

a second current mirror connected to said second voltage reference and to said first input terminal, as well as to a circuit node;

a third current mirror connected to said second voltage reference and to said second input terminal, as well as to said output terminal; and

a fourth current mirror connected to said first voltage reference, to said circuit node, as well as to said output terminal.

5. (Previously Presented) A signal receiver according to claim 4, wherein said conversion signal further comprises a current-voltage converter, inserted between said first and second voltage references and connected to said output terminal.

6. (Previously Presented) A signal receiver according to claim 4, wherein said conversion stage further comprises a resistive bridge connected to said input terminals, as well as to said first, second and third current mirrors.

7. (Previously Presented) A signal receiver according to claim 4, wherein said first current mirror comprises a first, second and third transistor inserted, in parallel to each other, between said first voltage reference and said first input terminal of said conversion stage, said bias terminal and said second input terminal of said conversion stage respectively, and having control terminals connected to each other, said second transistor being diode-configured.

8. (Previously Presented) A signal receiver according to claim 4, wherein said second current mirror comprises a fourth and a fifth transistor inserted, in parallel to each other, between said second voltage reference and respectively said first input terminal of said conversion stage and said circuit node, and having control terminals connected to each other, said fourth transistor being diode-configured.

9. (Previously Presented) A signal receiver according to claim 4, wherein said third current mirror comprises a sixth and a seventh transistor inserted, in parallel to each other, between said second voltage reference and respectively said second input terminal and said output terminal of said conversion stage and having control terminals connected to each other, said sixth transistor being diode-configured.

10. (Previously Presented) A signal receiver according to claim 4, wherein said fourth current mirror comprises an eighth and a ninth transistor inserted, in parallel to each other, between said first voltage reference and respectively said circuit node and said output terminal of said conversion stage and having control terminals connected to each other, said eighth transistor being diode-configured.

11. (Previously Presented) A signal receiver according to claim 5, wherein said current-voltage converter comprises a tenth and an eleventh transistor being inserted between said first voltage reference and said output terminal of said conversion stage and having a control terminal connected to said output terminal of said conversion stage and said eleventh transistor being inserted between said output terminal and said second voltage reference and having a control terminal connected to said output terminal of said conversion stage.

12. (Previously Presented) A signal receiver according to claim 6, wherein said resistive bridge comprises a first resistor connected to said first current mirror and, by means of a second resistor, to said first input terminal of said conversion stage, a third resistor connected to said first current mirror and, by means of a fourth resistor, to said second input terminal of said conversion stage, a fifth resistor connected to said second current mirror and, by means of said second resistor, to said first input terminal of said conversion stage, and a sixth resistor connected to said third current mirror and, by means of said fourth resistor, to said second input terminal of said conversion stage.

13. (Previously Presented) A signal receiver according to claim 12, wherein said resistive bridge further comprises a seventh resistor connected to said first and second input terminals of said conversion stage.

14. (Previously Presented) A signal receiver according to claim 4, wherein said first, second, third, eighth, ninth and tenth transistors are P-channel MOS transistors and in that said fourth, fifth, sixth, seventh and eleventh transistors are N-channel MOS transistors.

15. (Previously Presented) A signal receiver according to claim 4, wherein it comprises respective first and second capacities inserted between said first and second input terminals of said conversion stage and said first and second input terminals of said signal receiver.

16. (Previously Presented) A signal receiver according to claim 4, wherein said hysteresis comparator is a Schmitt trigger.

17. (Cancelled)

18. (Previously Presented) A digital signal receiver, comprising:

a converter having first and second input terminals adapted to receive respective input signals and a bias input adapted to receive a bias current, the converter operable to develop an intermediate signal on an intermediate output in response to the input signals and the intermediate signal having a hysteresis that is a function of the bias current; and

a hysteresis comparator coupled to the intermediate output of the converter to receive the intermediate signal, and the hysteresis comparator operable to develop a trigger signal in response to the intermediate signal; and

wherein the converter further comprises a resistor bridge and a plurality of MOS transistors, the resistor bridge operable to reduce voltages of the input signals to levels appropriate for the MOS transistors and operable to match an input

impedance of the digital signal receiver at the input terminals to an input impedance of a source applying the input signals.

19. (Previously Presented) The digital signal receiver of claim 18 wherein the intermediate signal generated by the converter comprises a trapezoidal signal independent of noise on the input signals.

20. (Previously Presented) The digital signal receiver of claim 18 wherein the converter comprises:

a first current mirror adapted to receive a first voltage reference and being coupled to the input terminals and coupled to the bias input;

a second current mirror adapted to receive a second voltage reference and being coupled to the first input terminal and coupled to an internal node;

a third current mirror adapted to receive the second voltage reference and being coupled to the second input terminal and coupled to the intermediate output; and

a fourth current mirror adapted to receive the first voltage reference and being coupled to the internal node and to the intermediate output.

21. (Previously Presented) The digital signal receiver of claim 20 wherein the converter further comprises a current-to-voltage converter coupled to the third and fourth current mirrors and operable to develop the intermediate signal responsive to third and fourth currents received from the third and fourth current mirrors, respectively.

22. (Previously Presented) The digital signal receiver of claim 21 wherein the current-to-voltage converter comprises two diode-coupled transistors having characteristics that may be varied to adjust the hysteresis of the converter.

23. (Previously Presented) An integrated circuit, comprising:

a digital signal receiver, including,

a converter having first and second input terminals adapted to receive respective input signals and a bias input adapted to receive a bias current, the converter operable to develop an intermediate signal on an intermediate output in response to the input signals and the intermediate signal having a hysteresis that is a function of the bias current; and

a hysteresis comparator coupled to the intermediate output of the converter to receive the intermediate signal, and the hysteresis comparator operable to develop a trigger signal in response to the intermediate signal; and

wherein the converter further comprises a resistor bridge and a plurality of MOS transistors, the resistor bridge operable to reduce voltages of the input signals to levels appropriate for the MOS transistors and operable to match an input impedance of the digital signal receiver at the input terminals to an input impedance of a source applying the input signals.

24. (Previously Presented) The integrated circuit of claim 23 wherein the integrated circuit comprises a digital signal processor operable to process the trigger signal from the digital signal receiver.

25. (Previously Presented) An electronic system, comprising:

an integrated circuit including a digital signal receiver, the digital signal receiver including,

a converter having first and second input terminals adapted to receive respective input signals and a bias input adapted to receive a bias current, the converter operable to develop an intermediate signal on an intermediate output in response to the input signals and the intermediate signal having a hysteresis that is a function of the bias current; and

a hysteresis comparator coupled to the intermediate output of the converter to receive the intermediate signal, and the hysteresis comparator operable to develop a trigger signal in response to the intermediate signal; and

wherein the converter further comprises a resistor bridge and a plurality of MOS transistors, the resistor bridge operable to reduce voltages of the input signals to levels appropriate for the MOS transistors and operable to match an input impedance of the digital signal receiver at the input terminals to an input impedance of a source applying the input signals.

26. (Previously Presented) The electronic system of claim 25 wherein the electronic system comprises a computer system.

27-30. (Cancelled)

31. (Previously Presented) A signal receiver inserted between a first and a second voltage reference and having a first and a second input terminal effective to receive differential signals and an output terminal effective to provide a converted signal, the signal receiver comprising:

a hysteresis comparator including an input terminal, the hysteresis comparator being connected to said output terminal of said signal receiver;

a conversion stage inserted between said first and second voltage references and connected between said first and second input terminals of said signal receiver and the input terminal of the hysteresis comparator, connected in turn to said output terminal of said signal receiver, said conversion stage performing a conversion from any input signal received on respective input terminals to an intermediate signal provided on an output terminal and suitable for reception by said hysteresis comparator;

wherein said conversion stage comprises:

a first current mirror connected to said first voltage reference and to said input terminals, as well as to said bias terminal;

a second current mirror connected to said second voltage reference and to said first input terminal, as well as to a circuit node;

a third current mirror connected to said second voltage reference and to said second input terminal, as well as to said output terminal; and

a fourth current mirror connected to said first voltage reference, to said circuit node, as well as to said output terminal;

wherein the second and third current mirrors are coupled to the first and second input terminals, respectively, through a resistor bridge operable to reduce voltages of the input signals to appropriate for a plurality of MOS transistors and operable to match an input impedance of the digital signal receiver at the input terminals to an input impedance of a source applying the input signals.